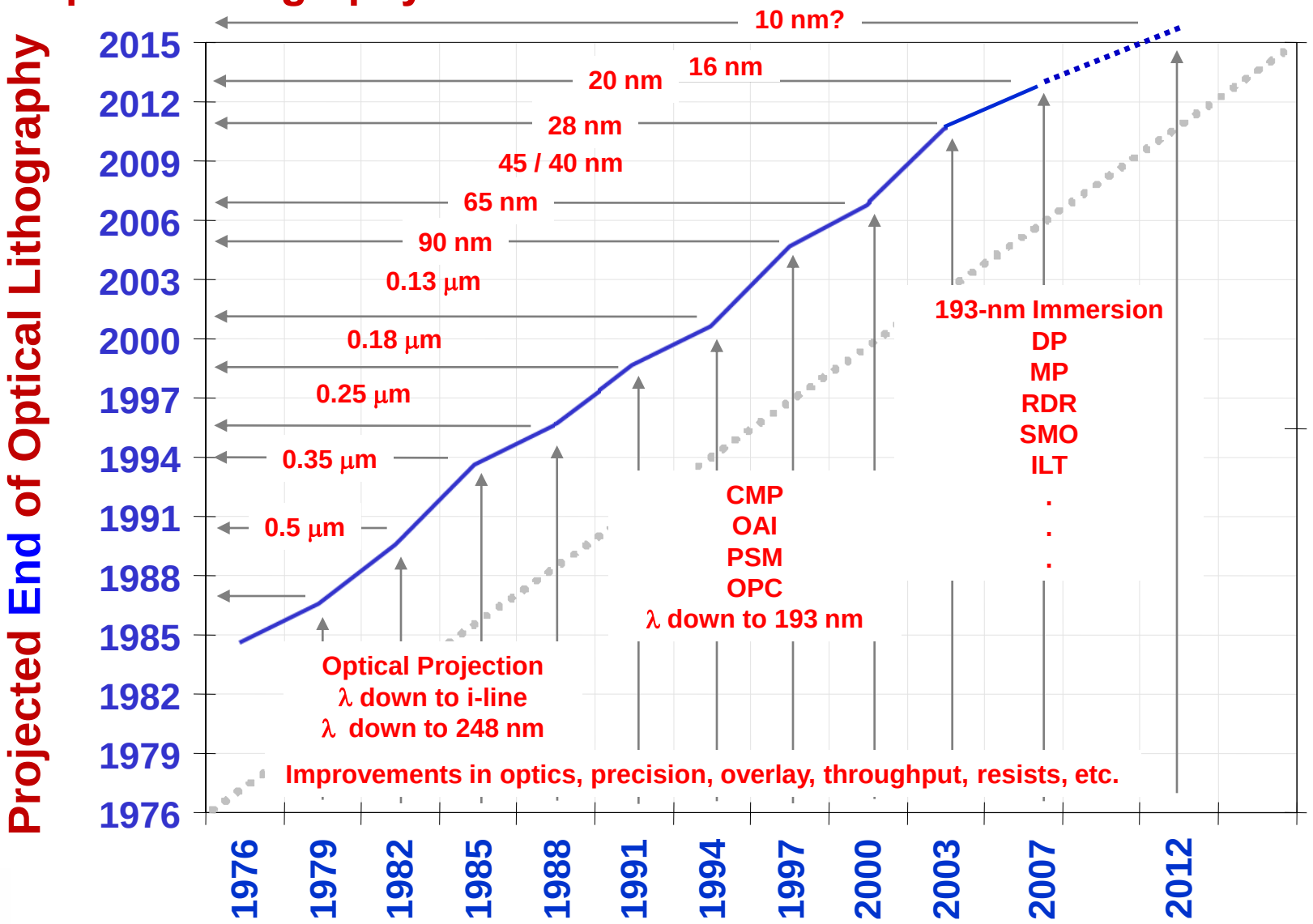
Mask Technology Development in Extreme-Ultraviolet Lithography

Anthony Yen

September 6, 2013

Optical lithography has sustained Moore's law for ~ 5 decades

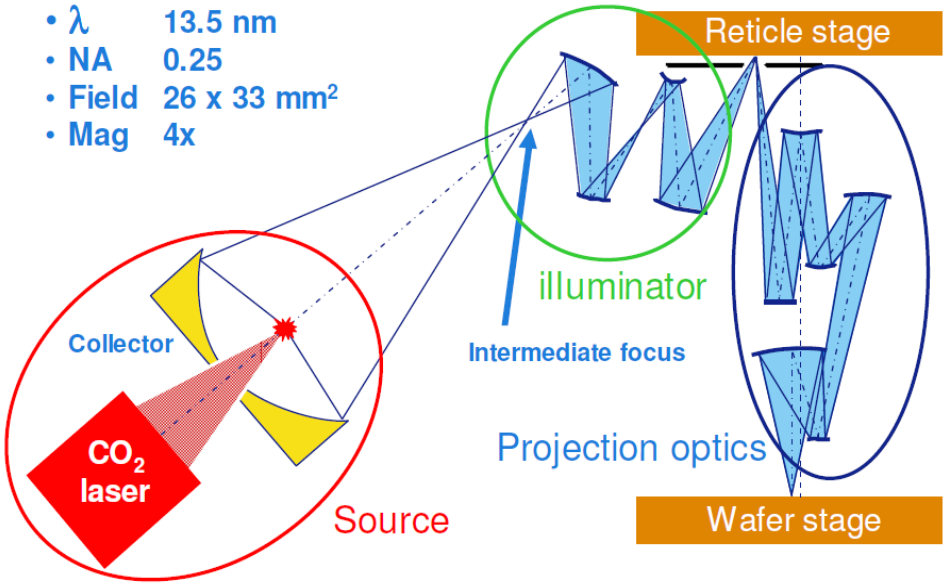


J. Sturtevant, B.J. Lin, A. Yen

EUV Lithography in Practice

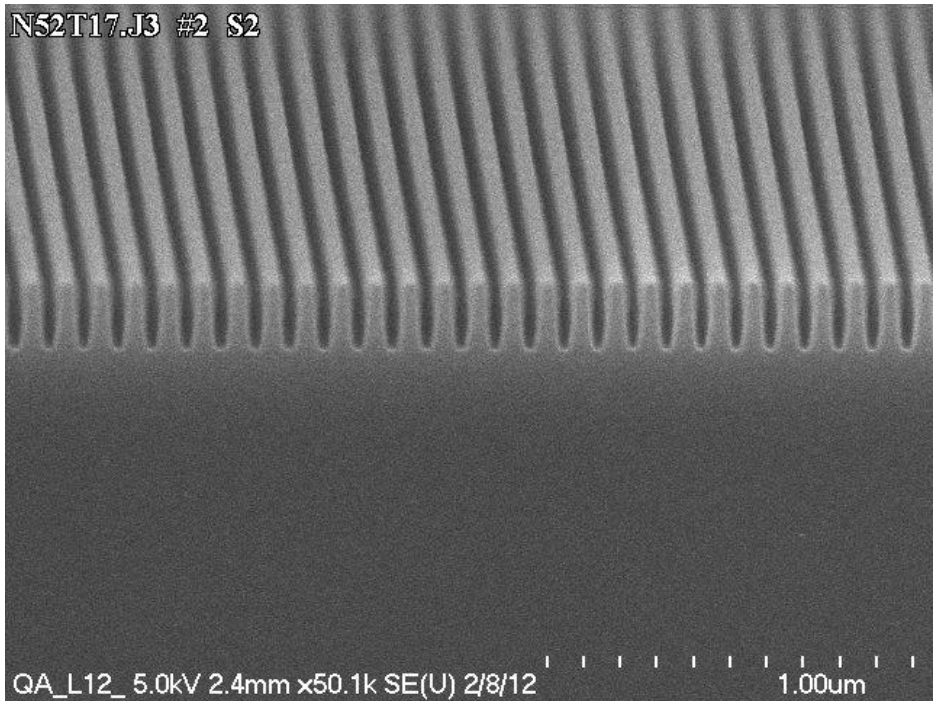
NXE3100 EUV scanner exposing wafers at TSMC since Nov 2011

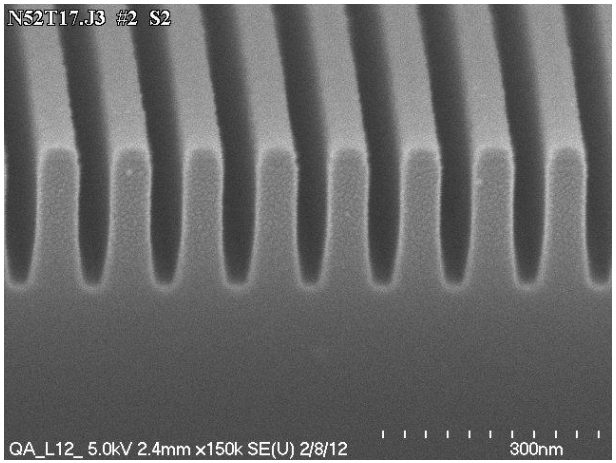
- λ 13.5 nm
- NA 0.25
- Field 26 x 33 mm²
- Mag 4x



Throughput : 8 wph using ASML's ATP procedure

EUV definition of spaces etched into silicon

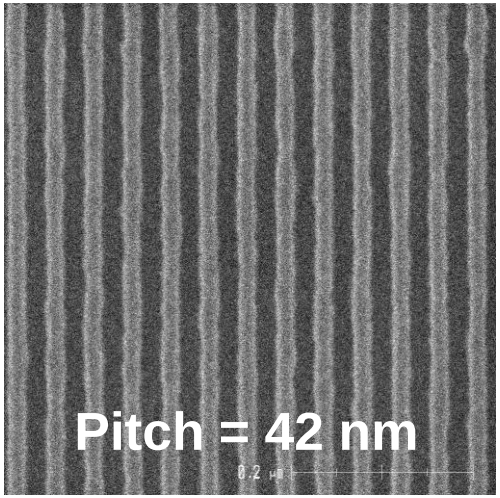


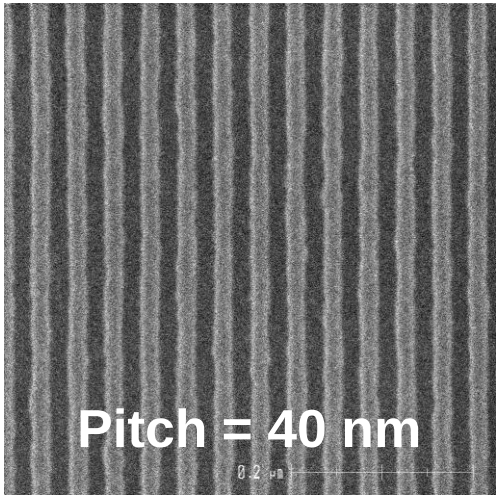


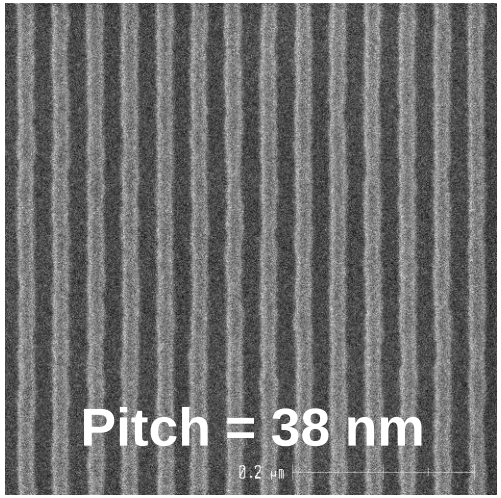
Pitch = 46 nm; NA = 0.25; quadrupole illumination

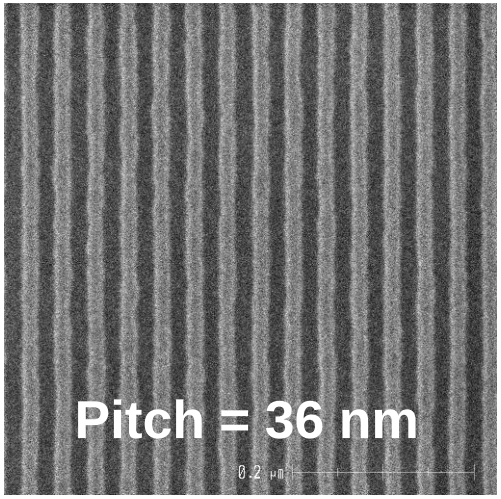
Resolution Limit of NXE3100

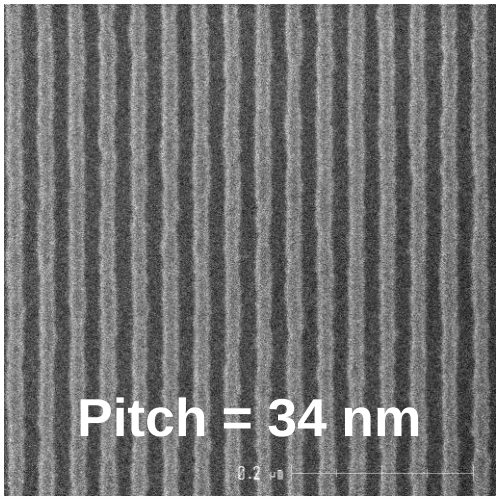
with dipole illumination

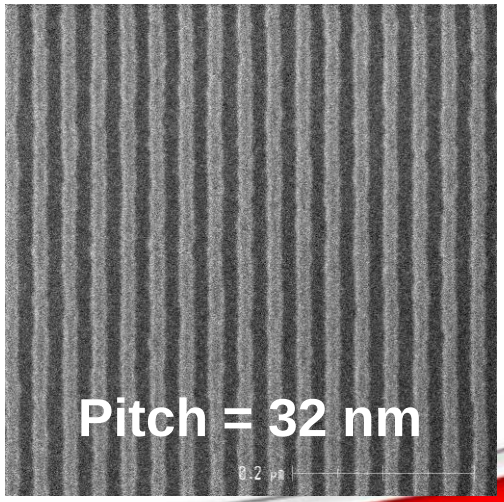




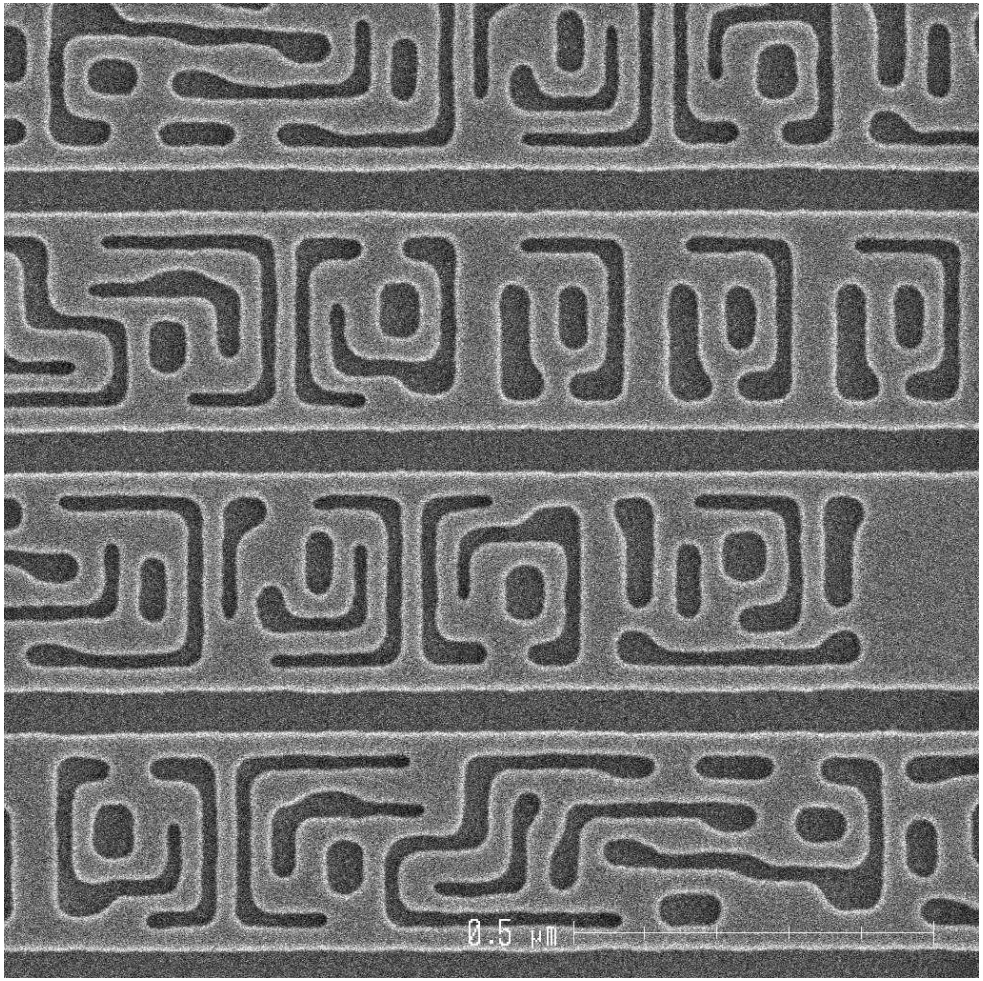






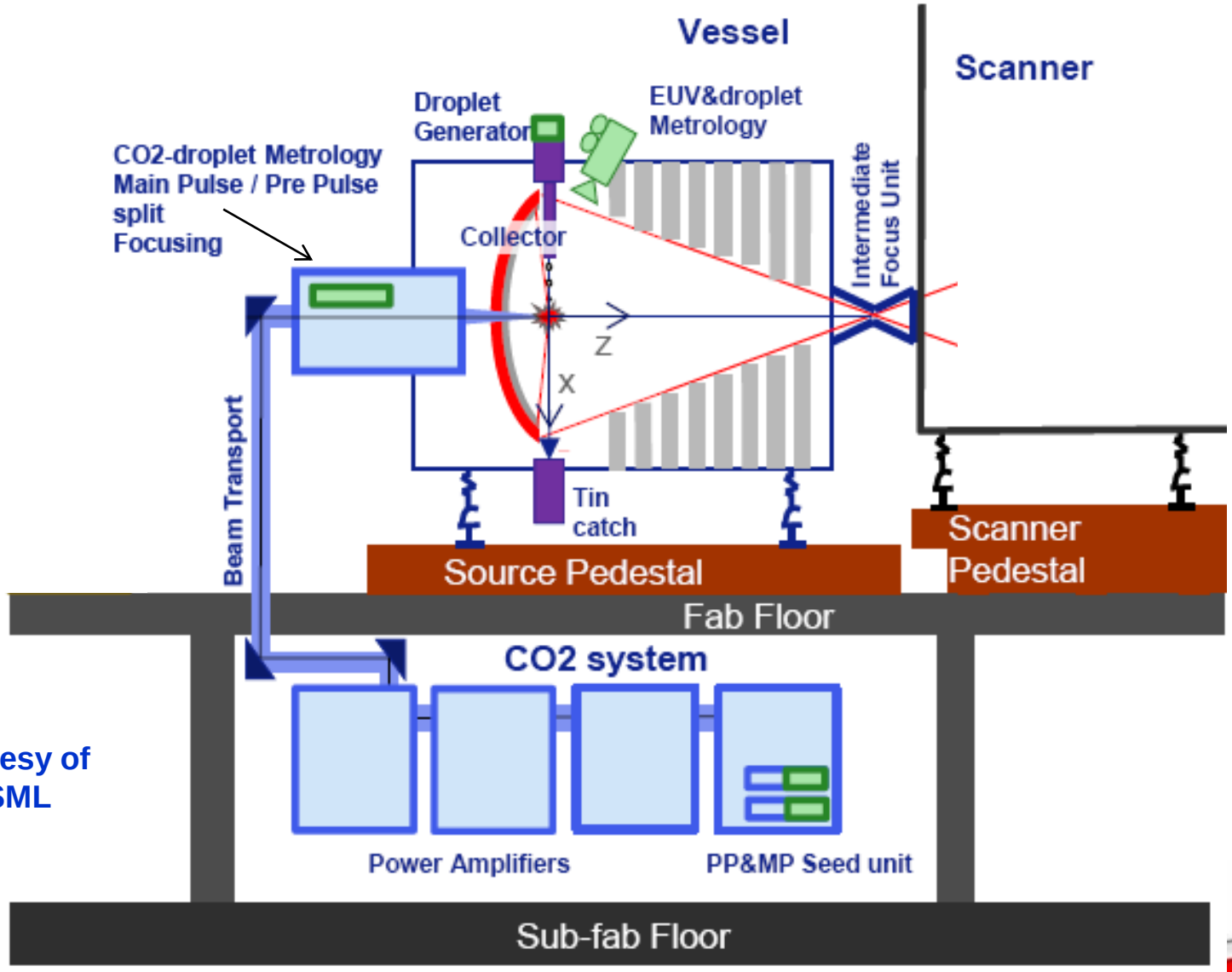


EUV processing of metal layer of logic circuit



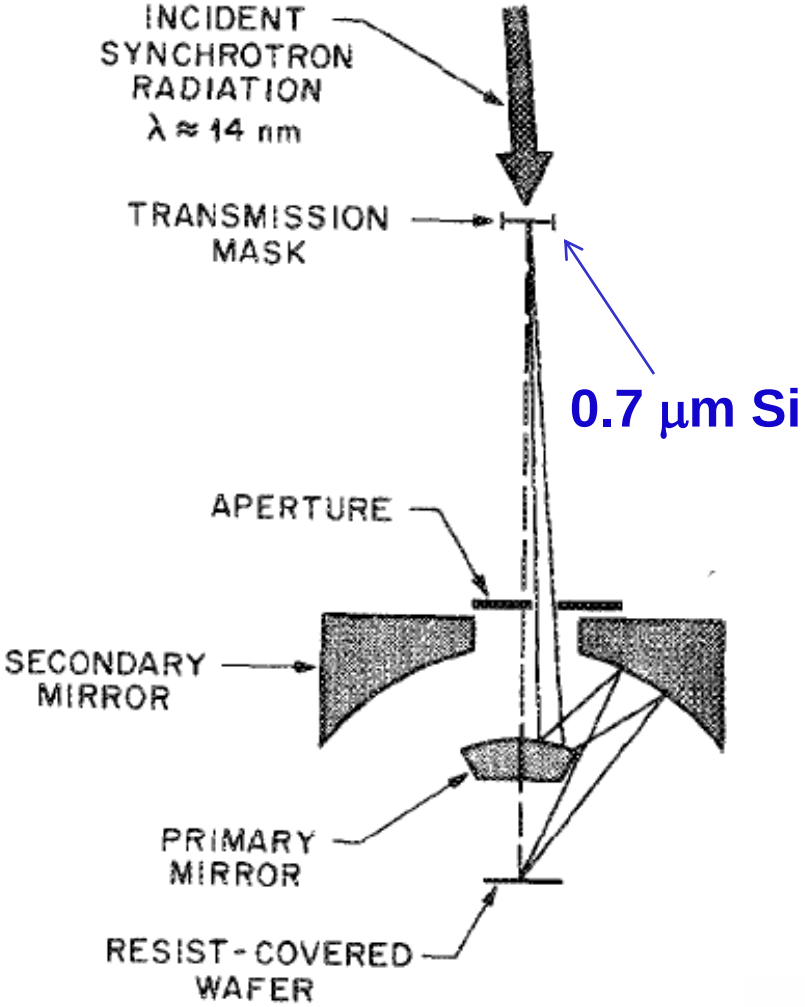
After hard-mask etch-through

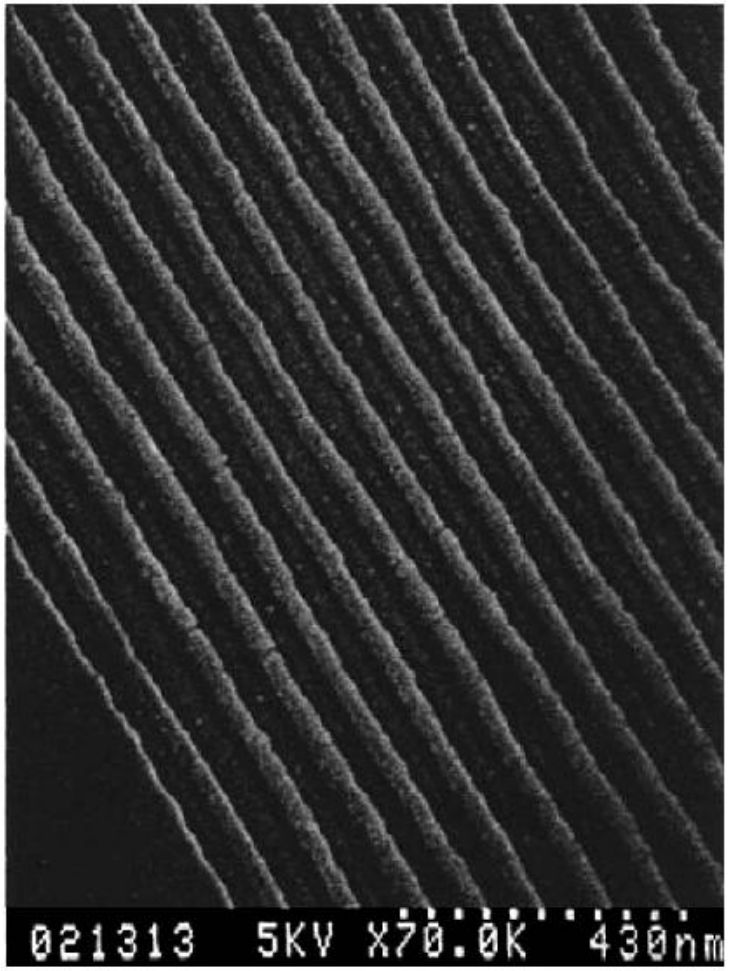
Laser-Produced Plasma EUV Source



Courtesy of ASML

Early EUV Lithography Used Membrane Mask



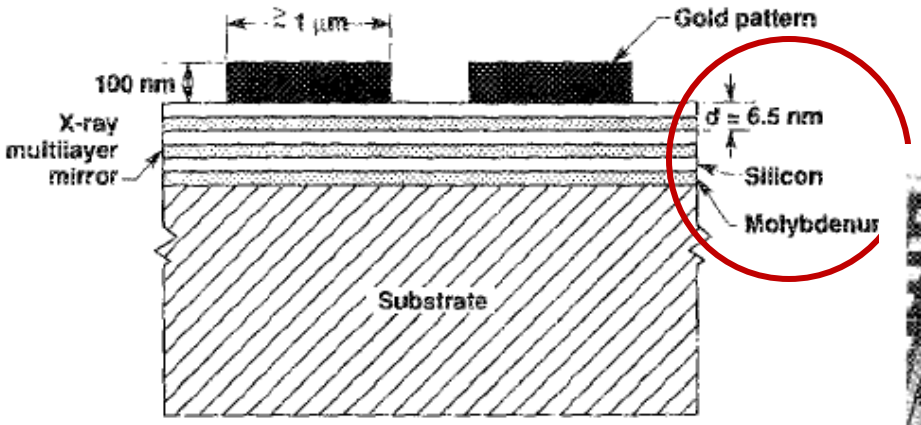


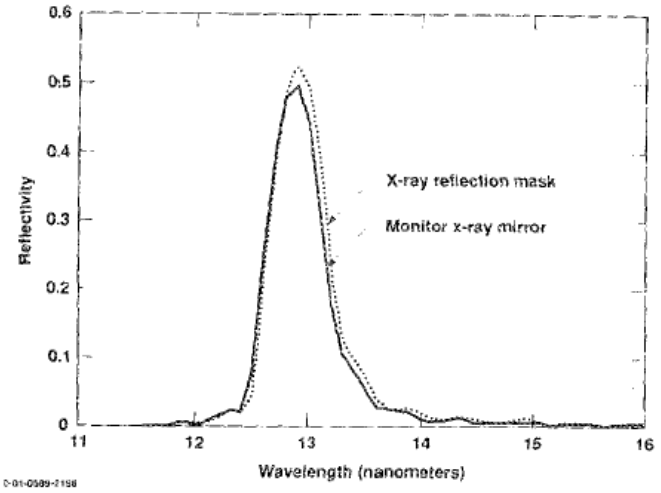
NA = 0.08

Pitch = 100 nm

Bjorkholm et al., JVST B 8, 1509, Nov/Dec 1990

Reflective Mask Was Proposed and Fabricated





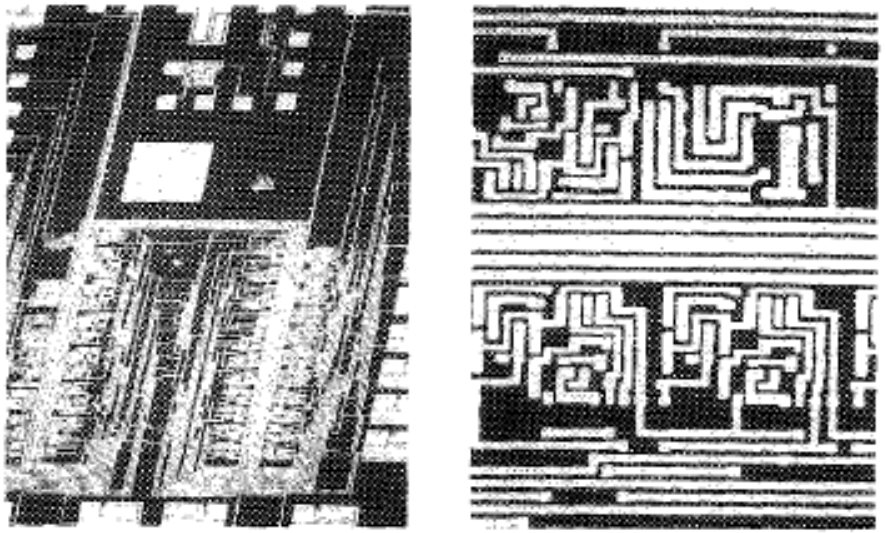


FIG. 3. Scanning electron micrographs of an XRPL mask. The bright regions are areas of 100 nm thick gold, patterned onto a soft x-ray multilayer mirror.

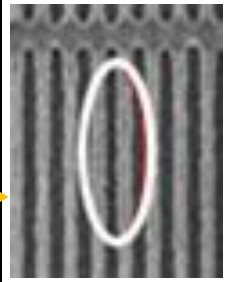
Hawryluk et al., JVST B7, 1702, Nov/Dec 1989

Patterned-EUV-mask Inspection

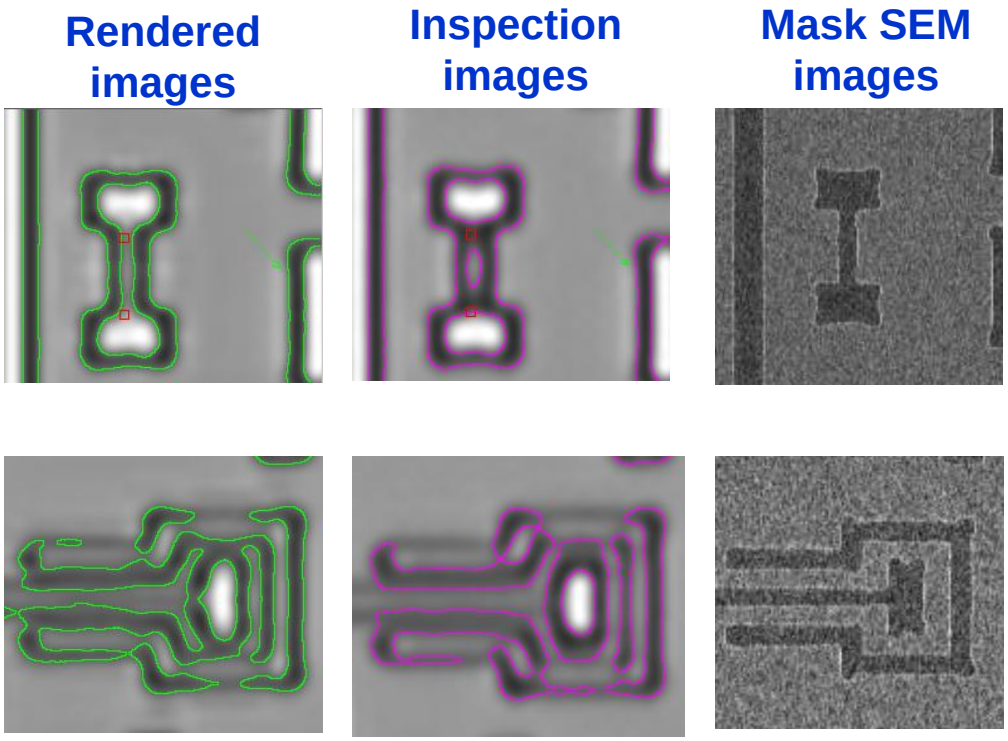
Detection resolution of a DUV inspector

Pattern shift		Programmed defect size on mask (nm)	4	5	6	7	8	9	10	11	12	13	14	15	16	X
		High-sensitivity setting														
		Low-sensitivity setting														
CD-over		Programmed defect size on mask (nm)	6	8	10	12	14	16	18	20	22	24	26	28	30	X
		High-sensitivity setting														
		Low-sensitivity setting														
CD-under		Programmed defect size on mask (nm)	-6	-8	-10	-12	-14	-16	-18	-20	-22	-24	-26	-28	-30	X
		High-sensitivity setting														
		Low-sensitivity setting														
Extursion		Programmed defect size on mask (nm)	56	64	72	80	88	96	104	112	120	128	136	144	152	X
		High-sensitivity setting														
		Low-sensitivity setting														
Pin-hole		Programmed defect size on mask (nm)	28	32	36	40	44	48	52	56	60	64	68	72	76	X
		High-sensitivity setting														
		Low-sensitivity setting														
Intrusion		Programmed defect size on mask (nm)	56	64	72	80	88	96	104	112	120	128	136	144	152	X
		High-sensitivity setting														
		Low-sensitivity setting														
Pin-dot		Programmed defect size on mask (nm)	28	32	36	40	44	48	52	56	60	64	68	72	76	X
		High-sensitivity setting														
		Low-sensitivity setting														

SEM image on wafer

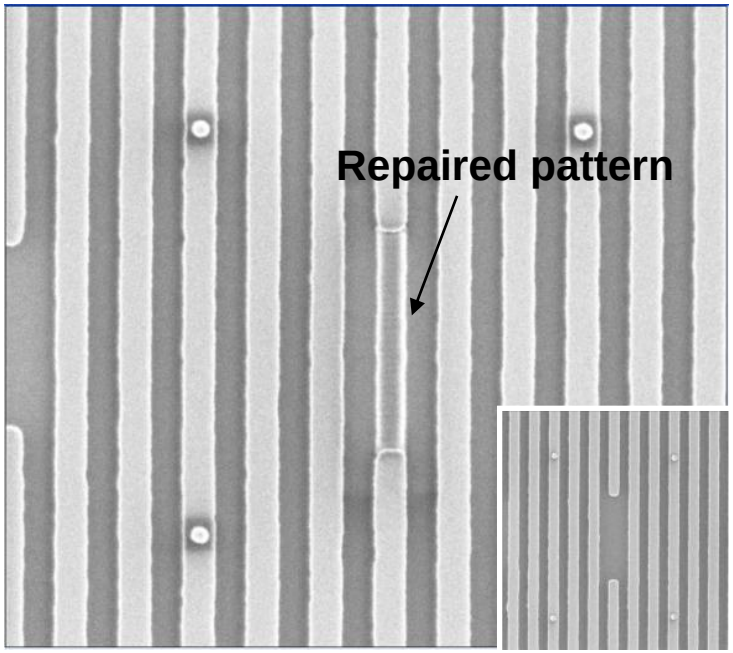


False defects in EUV mask pattern inspection

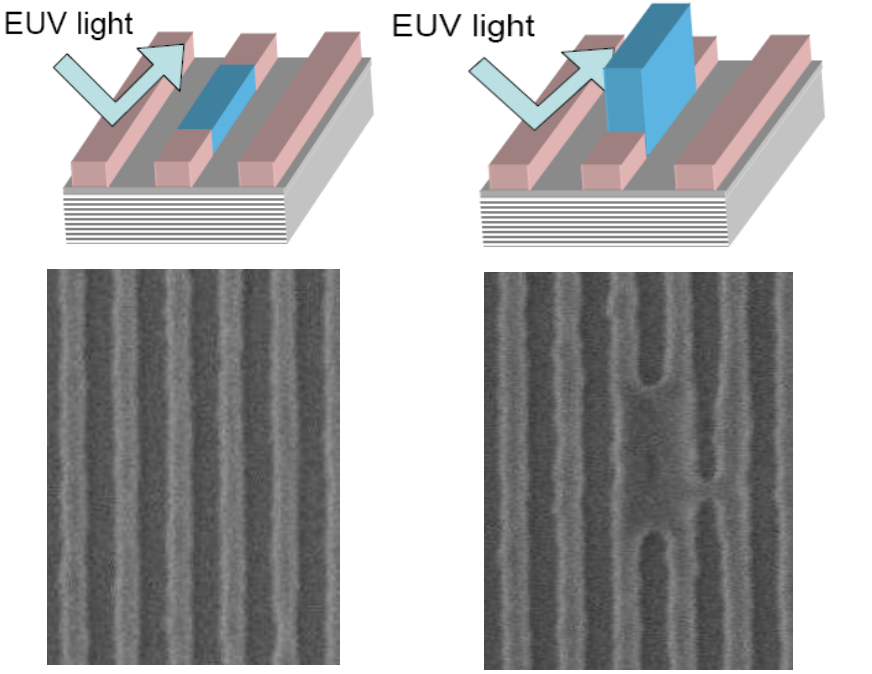


More accurate optical modeling is required for better image rendering to minimize false defects

3D profile control is key in EUV mask repair



Mask SEM image



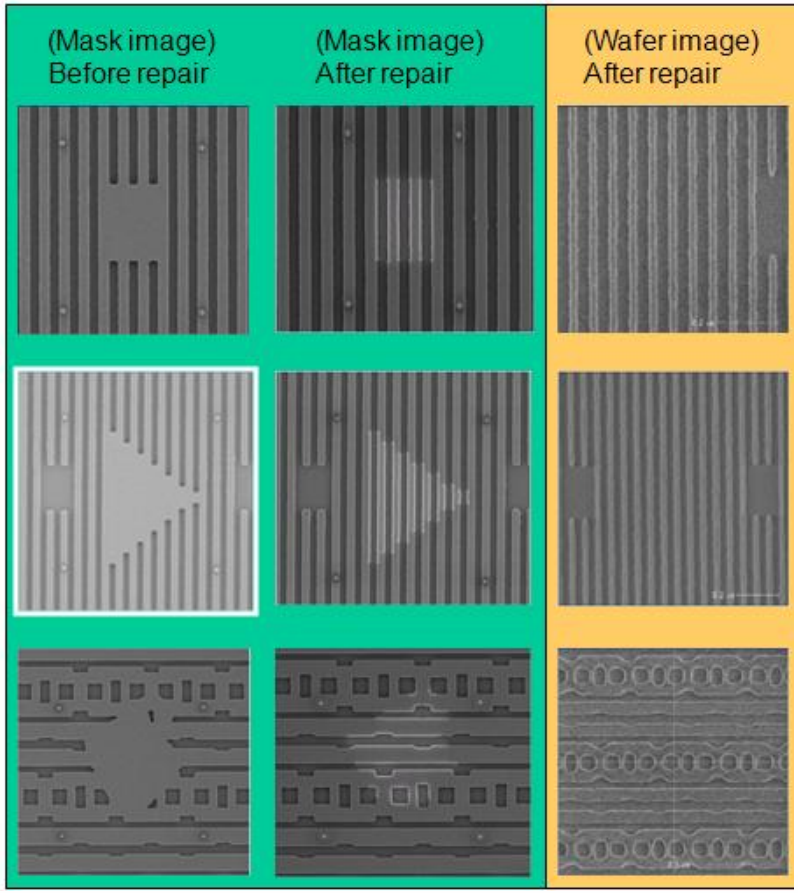
Perfectly repaired

Shadow effect is observed!

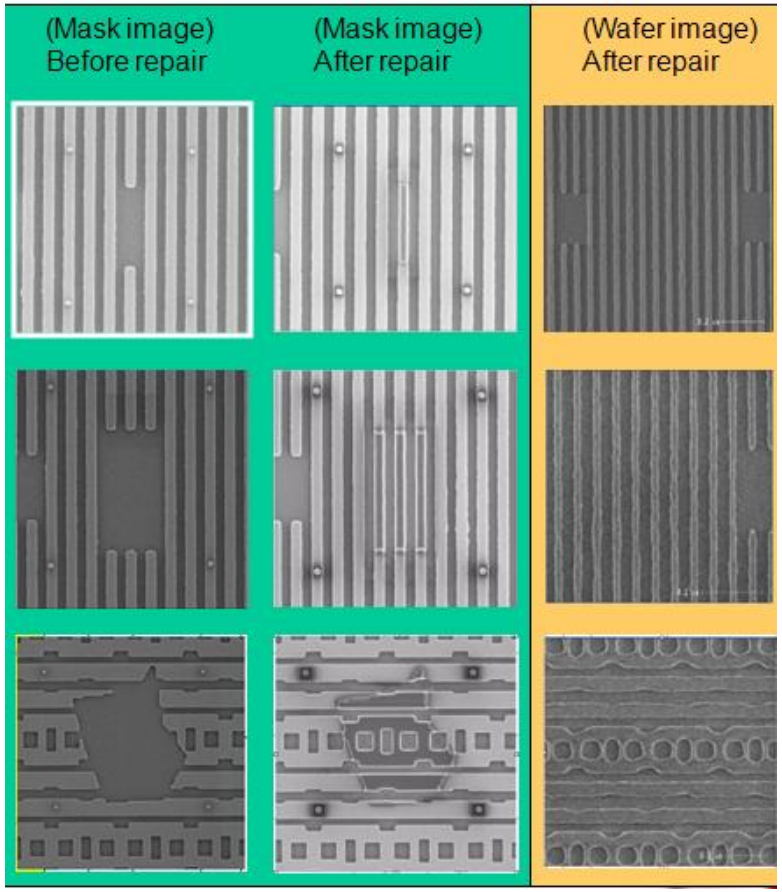
Wafer printing results

EUV absorber defects are repairable

Opaque Defects

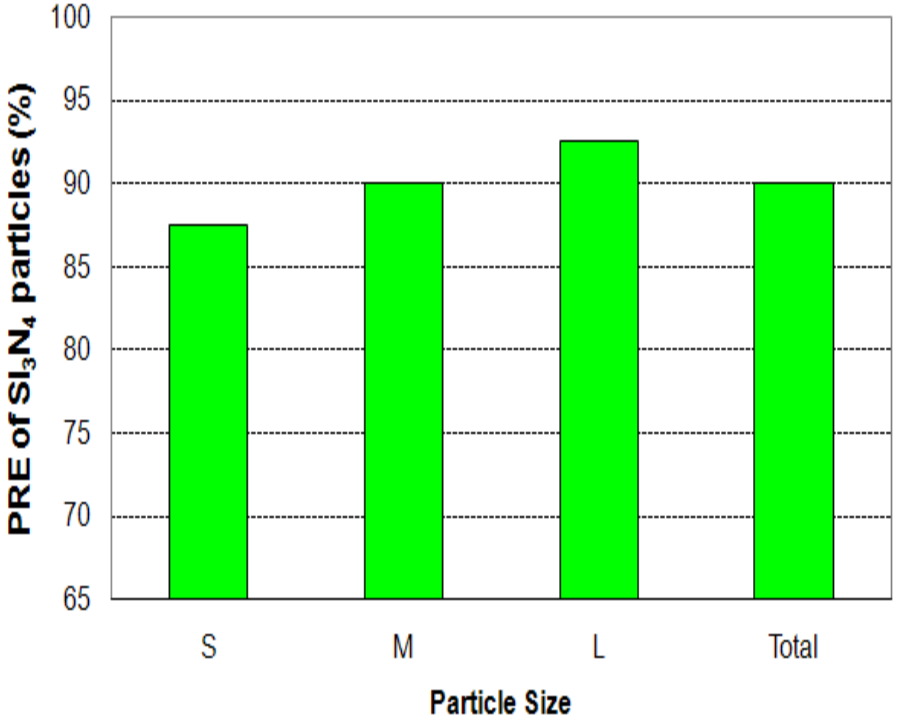


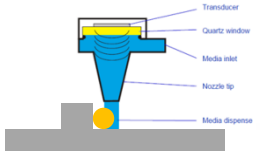
Clear (Missing) Defects



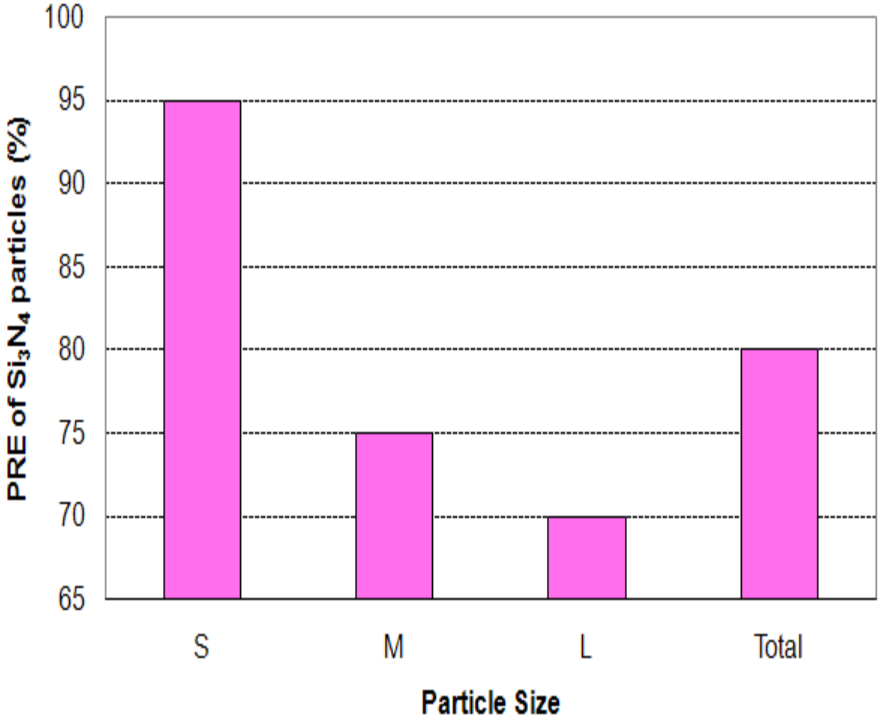
PRE enhancement in mask cleaning using complementary physical force

Spray Cleaning



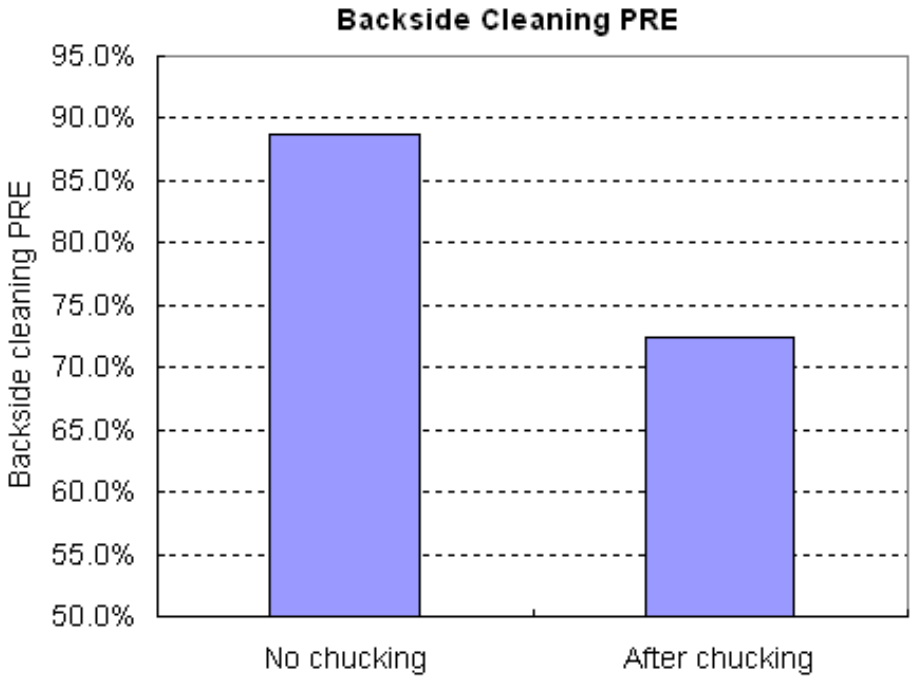


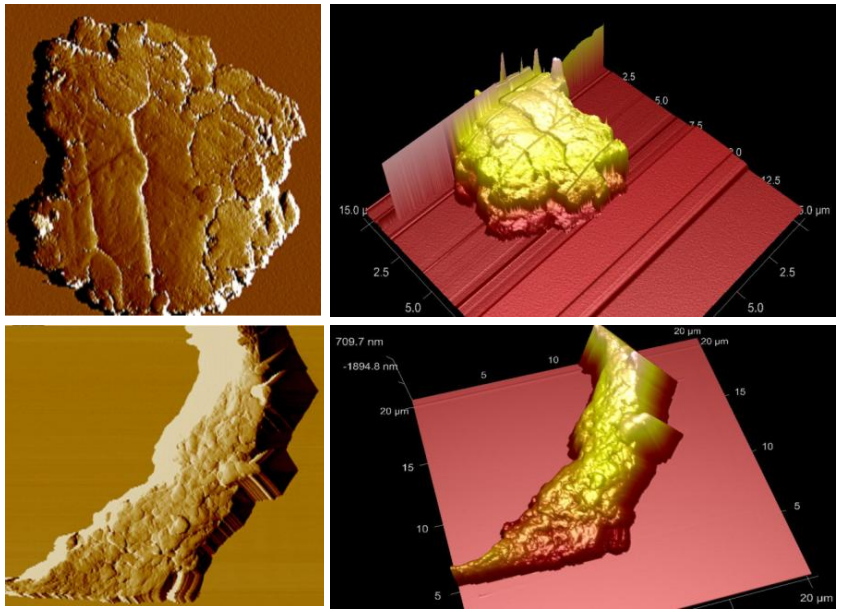
Megasonic Cleaning



Particle size S: 40~80 nm; M: 81~150 nm; L: >150 nm

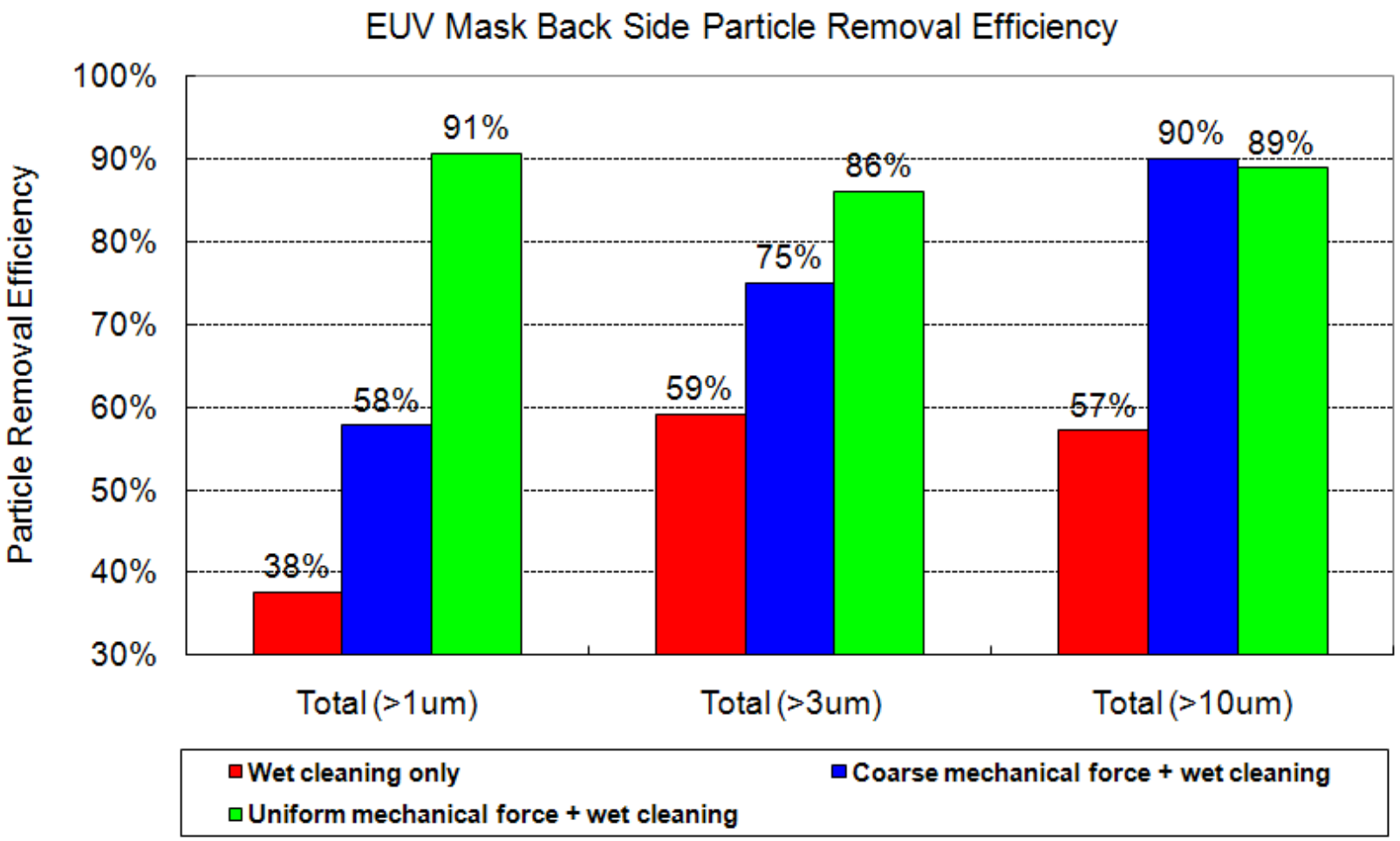
Conventional mask cleaning cannot easily remove compressed particles on the back side





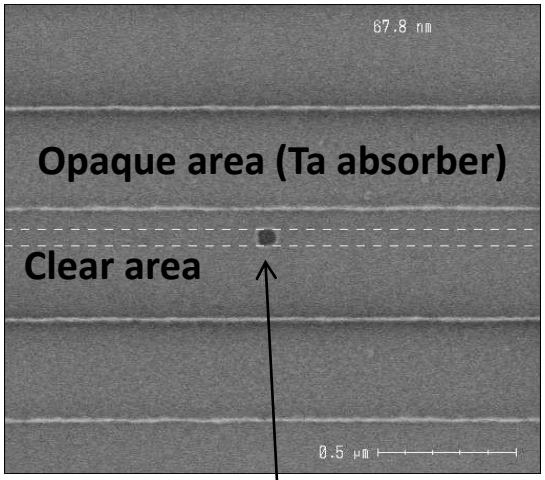
AFM images of post-chucking back-side particles

Mechanical-force cleaning of mask back side



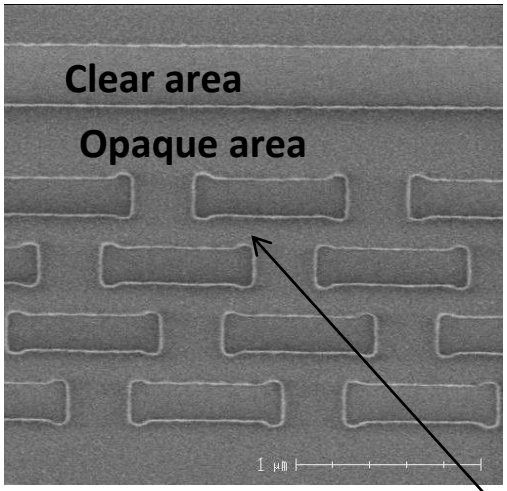
Mitigation of mask blank defects by a global shift of mask patterns

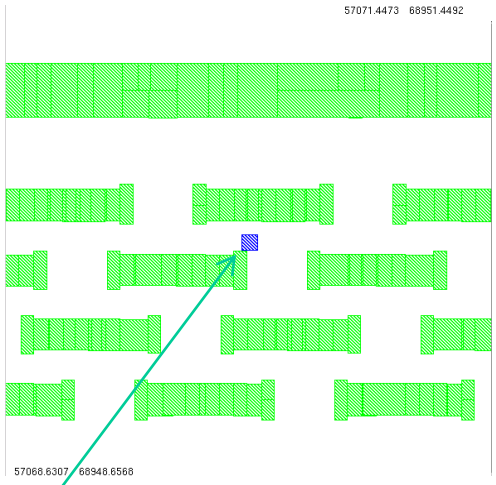
Without pattern shift



This blank defect (~70nm on mask) is in the clear area and will be printed on wafer

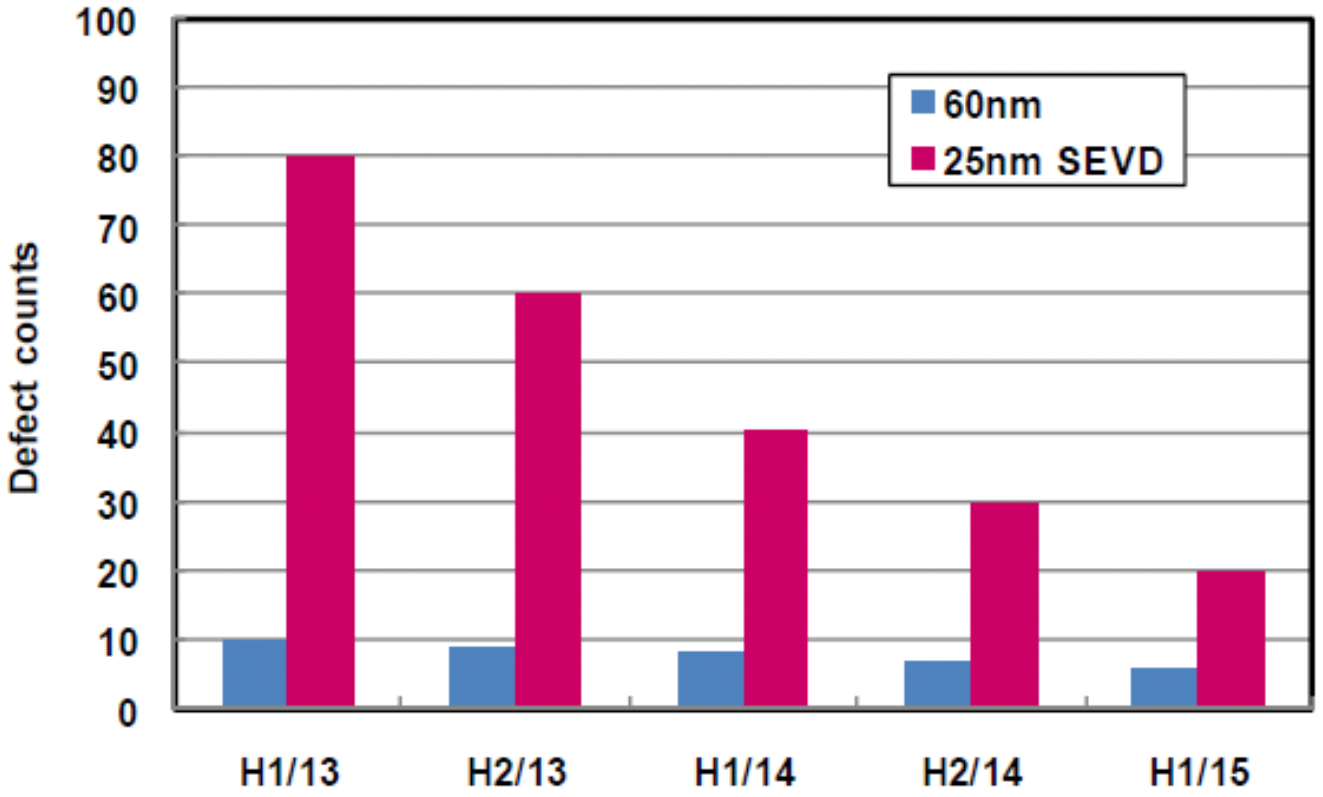
With pattern shift





After global pattern shift, a blank defect shown above is now hidden under the Ta absorber

EUV mask blank defect reduction roadmap

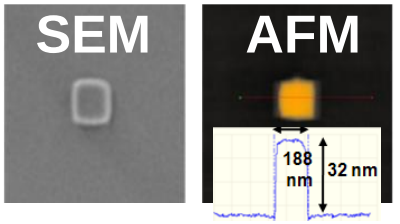


Courtesy of HOYA Corporation

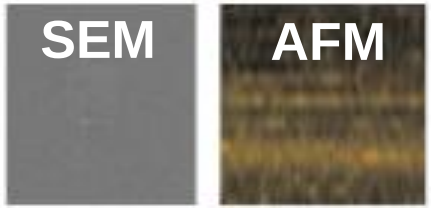
Use of Nano-machining and electron-beam mask repair tools to eliminate bumps and pits on LTEM substrates

Elimination of bump defect on LTEM

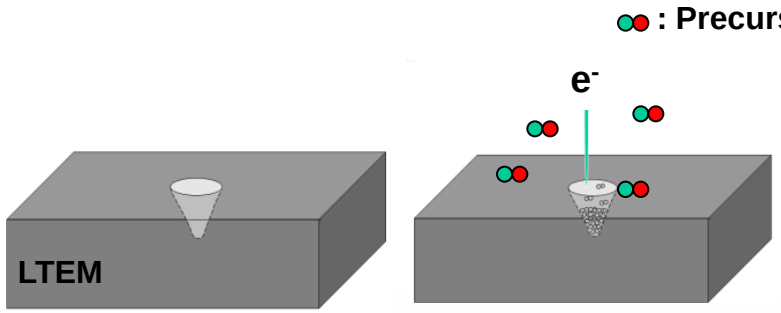
Before



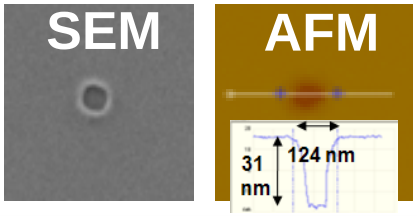
After



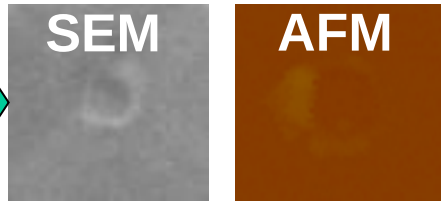
Elimination of pit defect on LTEM



Before

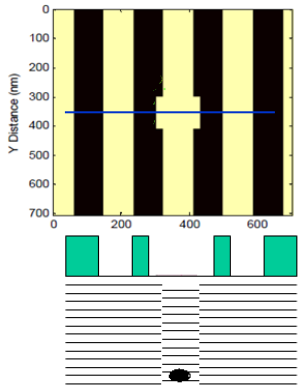


After



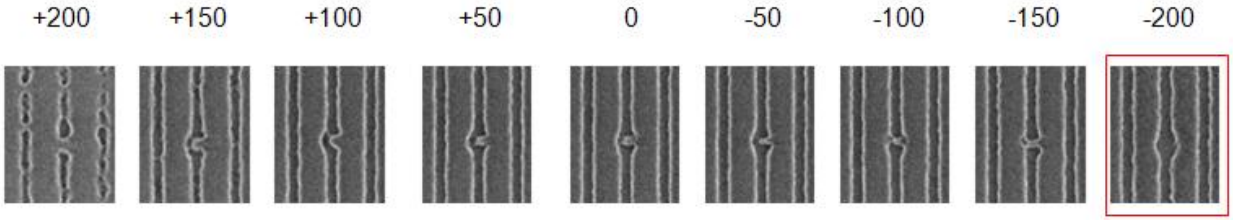
Compensation of mask blank defects

Absorber pattern on mask



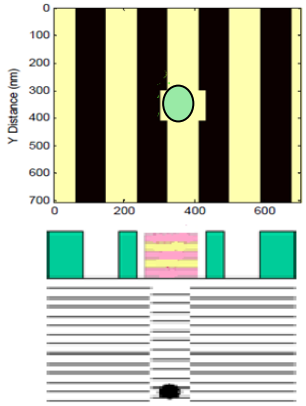
Cross Section

Usual compensation repair: wafer image



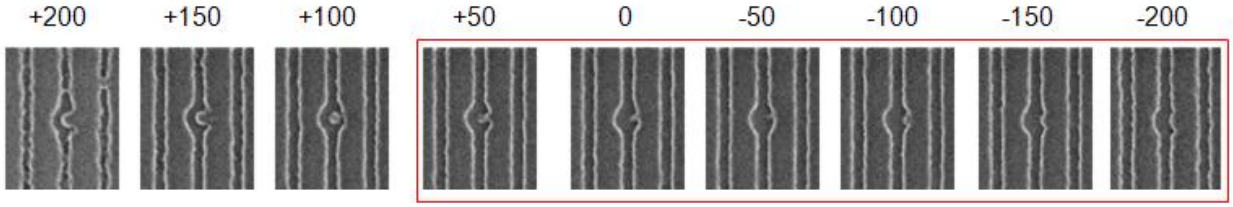
Defocus (nm)

Absorber patterns on mask



Cross section

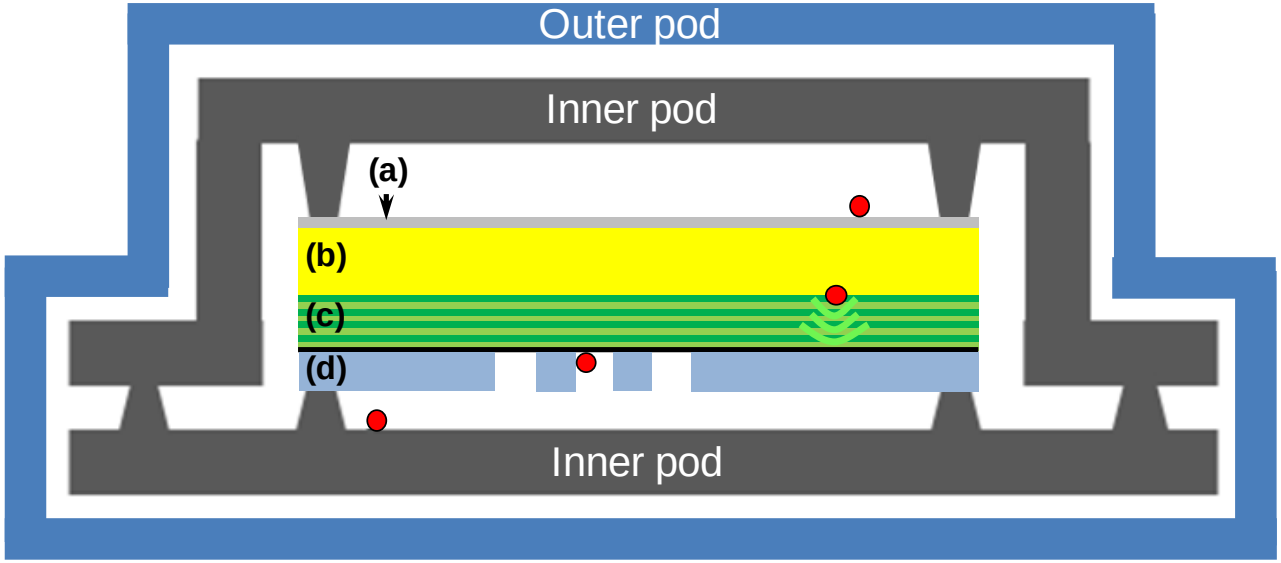
Novel compensation repair: wafer image



Defocus (nm)

Compensation repair aims to form a more tolerable image on wafer

EUV Mask in a Dual-Pod



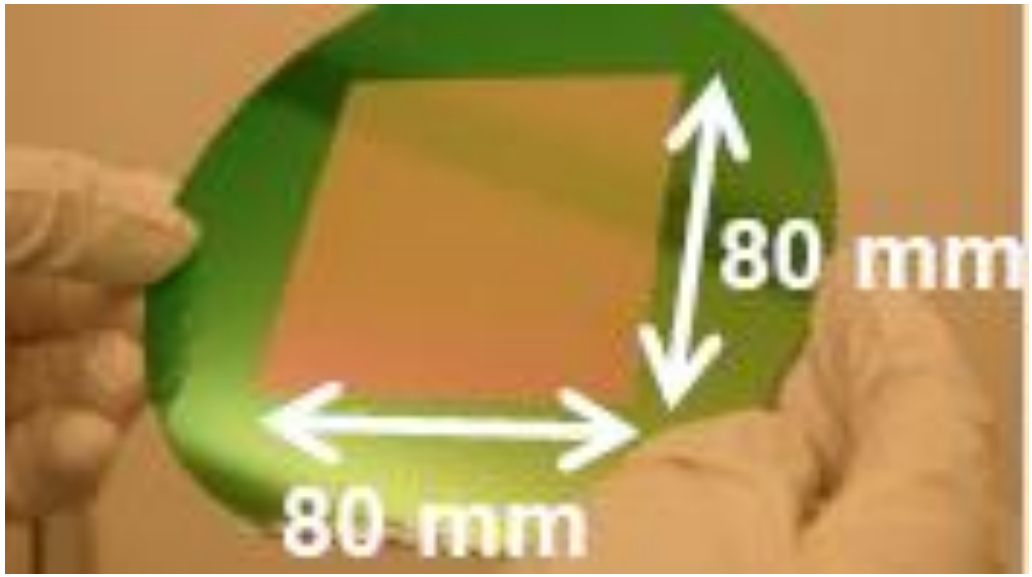
(a) Conductive layer

(b) Low thermal expansion material

(c) Mo/Si multilayer

(d) Absorber

Progress on Pellicles for EUV Masks



- 55 nm in thickness
- No support structure
- > 80% transparency

Courtesy of ASML

To Make EUV HVM a Reality

- Progress towards 250 W source power must not slow down
  - 250-W scanners should be operational in 2015
- Native defects in mask blanks must be further reduced by an order of magnitude
  - From best-case ~100 today to mostly ~10 (at ~30 nm in size)
  - Suppliers must make the necessary investments in new and dedicated processing tools for blank fabrication
- Continuous progress must take place on realizing EUV pellicles (110 x 145 mm in size)
  - Must be > 90% per-pass transparency
  - Potential commercial suppliers should seize this opportunity and not withdraw from the challenge